REMARKS

The specification has been objected to because the Abstract of the Disclosure refers to the current routine and total accessing times. The Abstract is amended to correct the language. It is believed that the objection is overcome, and reconsideration is requested.

The disclosure is objected to for certain formalities. In view of the amendments to the specification, it is believed that the objections are overcome.

Specifically, the amended paragraph on page 6, lines 8-12, has been amended as suggested by the Examiner. The amended paragraph at page 6, lines 13-20 has been amended as suggested by the Examiner. The amended paragraph at page 7, lines 5-12 has been amended as suggested by the Examiner. References to the "current iteration loop counter" have been changed to "current loop iteration counter" as suggested by the Examiner. References to "total iteration loop counter" have been changed to "total loop iteration count" as suggested by the Examiner. It is believed that all of the objections to the specification have been overcome, and reconsideration is requested.

The drawings are objected to for informalities. Regarding the objection to Figures 3 and 4, Figure 4 is amended to show that in Routine 1 instructions A and B are both executed 40 times. Also, Figure 5 is amended to replace "Current Access Loop Counter" with "Current Loop Iteration Counter" and to replace "Old Access Loop Counter" with Total Loop Iteration Count." Reconsideration of the objections to the drawings is requested. With regard to the objection to Figure 9, the reference numeral 230 has been changed to 220 to indicate the address trace cache in accordance with the invention. In view of the amendments to the drawings, it is believed that all objections to the drawings are overcome, and reconsideration is requested.

Claim 1 is objected to for certain informalities. The claim has been amended to address all of the informalities. Reconsideration is requested.

Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The claim is amended to distinguish the two types of routines executed in accordance with the

invention. Specifically, the claim is amended to recite first and second routines having first and second groups of instruction. The first routine is not repeatedly executed, and the address trace cache in the case of the first routine stores addresses corresponding to each instruction according to an order of executed instructions. The second routine is repeatedly executed, and the address trace cache in the case of the second routine stores a start address of the routine, an end address of the routine, a current iteration count of the routine representing a current number of executed iterations of the routine, and a total number of iterations of the routine. It is believed that the claim language has been clarified to distinguish the two types of routines. Reconsideration of the rejection of the claim under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Claim 1 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rotenberg, et al. In view of Kiuchi, et al. In view of the amendments to the claim and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The invention is directed to an address trace cache which employs two approaches to executing routines, depending on whether the routine is repeatedly executed, that is, whether it is a loop routine. In a first type of routine execution, the routine is executed only a single time. In this case, the addresses related to the instructions of the routine are stored in order in the address trace cache. When the second type of routine is to be executed repeatedly, the addresses of the instructions are not stored in order in the address trace cache. Instead, the routine start address the routine end address, the current number of executed iterations and the total number of iterations are stored in the address trace cache.

The claim is amended to more clearly set forth the features of the invention. That is, the claim is amended to specify a method of executing instructions using an address trace cache in which execution of a routine can be carried out in one of two possible fashions, depending on whether the routine is executed repeatedly or only a single time. Neither of Rotenberg, et al. and Kiuchi, et al. taken alone or in combination, teaches or suggests this feature of the invention, now clearly set forth in the amended claim.

Rotenberg, et al. teach an approach to using a trace cache. In the Rotenberg, et al. system, a single approach to executing instructions is employed. Specifically, instructions, not address, are stored in a trace cache in the order in which they are to be executed. There is no teaching or suggestion in Rotenberg, et al. of storing any types of addresses in an address trace cache, as the applicants claim. Furthermore, there is no teaching or suggestion in Rotenberg, et al. of using one or both of two possible approaches to executing instructions, depending on whether a routine is executed repeatedly. The approach to storing instructions is the same regardless of the routine being executed. That is, there is no teaching or suggestion in Rotenberg, et al. of storing addresses related to instructions of a routine in order in an address trace cache when the routine is executed once, and storing start and end addresses, current loop iteration and total number of iterations of the routine in the address trace cache when the routine is executed repeatedly.

Kiuchi et al. is directed to a system for handling execution of repeat instructions. Kiuchi, et al. is unrelated to an address trace cache. Also, there is no teaching or suggestion in Kiuchi, et al. of the applicants' claimed method using an address trace cache in which instructions of routines are executed differently depending on whether the routines are executed repeatedly.

Neither Rotenberg, et al. nor Kiuchi, et al. teach or suggest the applicants' claimed method of executing instructions using an address trace cache in which instructions of routines are accessed based on whether the routines are executed repeatedly. That is, there is no teaching or suggestion in Rotenberg, et al. or Kiuchi, et al. of using one or both of two possible approaches to executing instructions, depending on whether a routine is executed repeatedly. That is, there is no teaching or suggestion in either reference of storing addresses related to instructions of a routine in order in an address trace cache when the routine is executed once, and storing start and end addresses, current loop iteration and total number of iterations of the routine in the address trace cache when the routine is executed repeatedly.

Since neither reference provides such teaching or suggestion, there is no combination of the references which would result in providing such teaching or suggestion. Since, Rotenberg, et al. and Kiuchi, et al., taken alone or in combination, fail to teach or suggest the invention set

forth in the amended claim, it is believed that the claim is allowable over the cited references. Accordingly, reconsideration of the rejection of claim 1 under 35 U.S.C. § 103(a) based on Rotenberg, et al. and Kiuchi, et al. is respectfully requested.

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Fig. 4

(Prior Art)

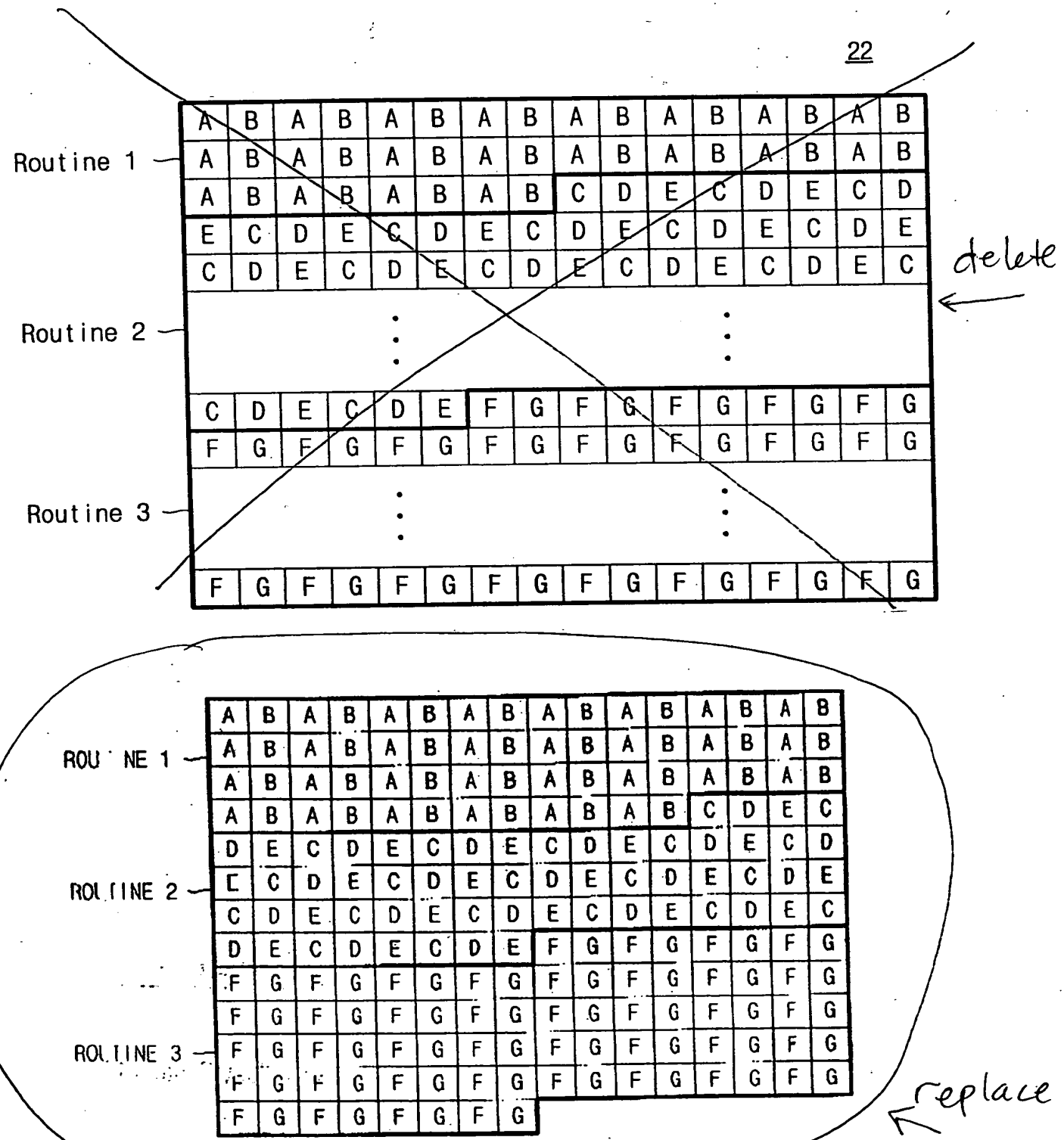

Fig. 5

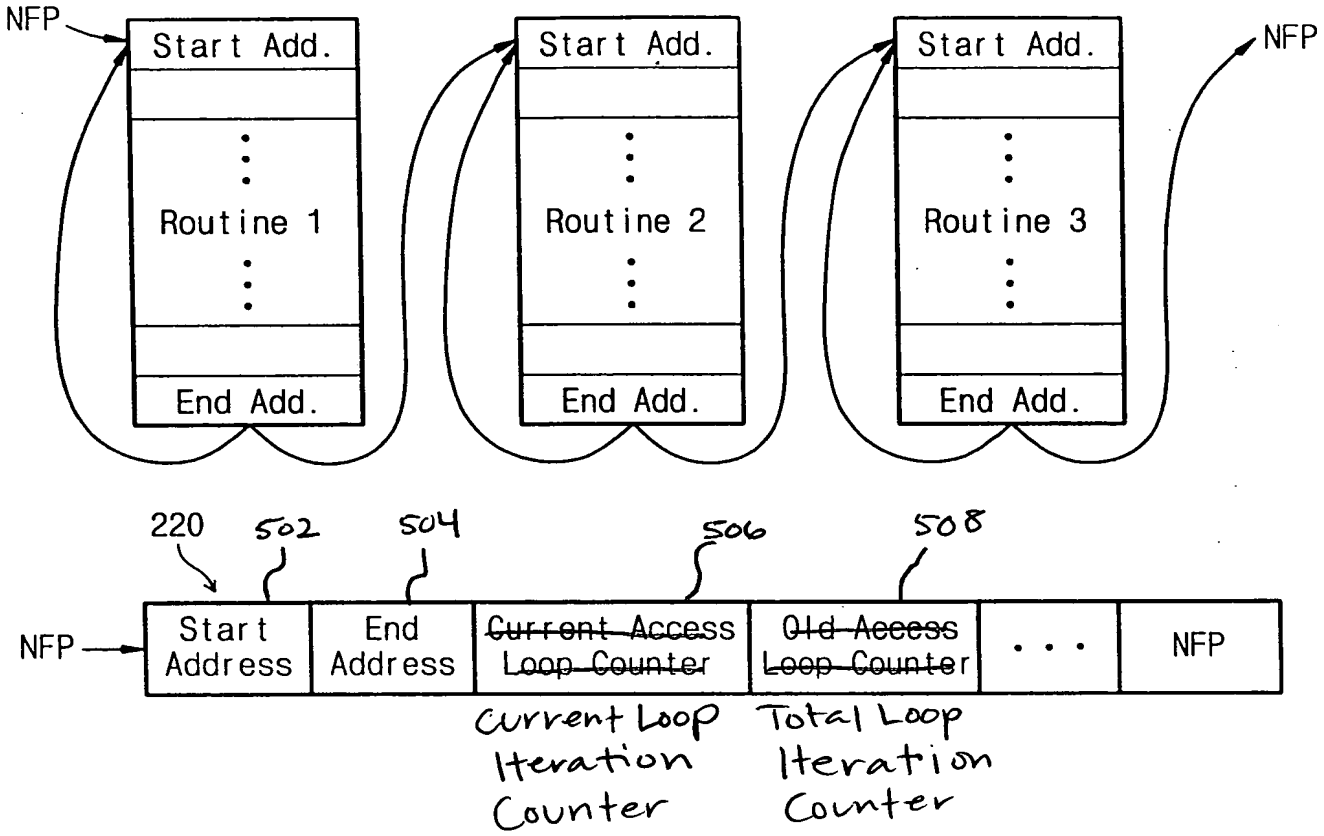

Fig. 6

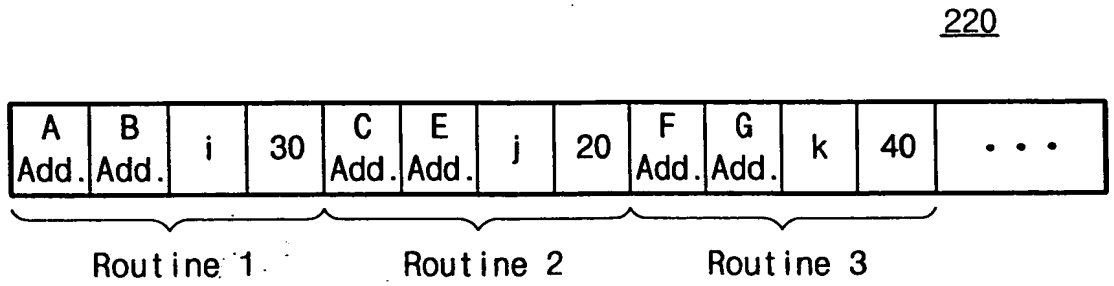

Fig. 8

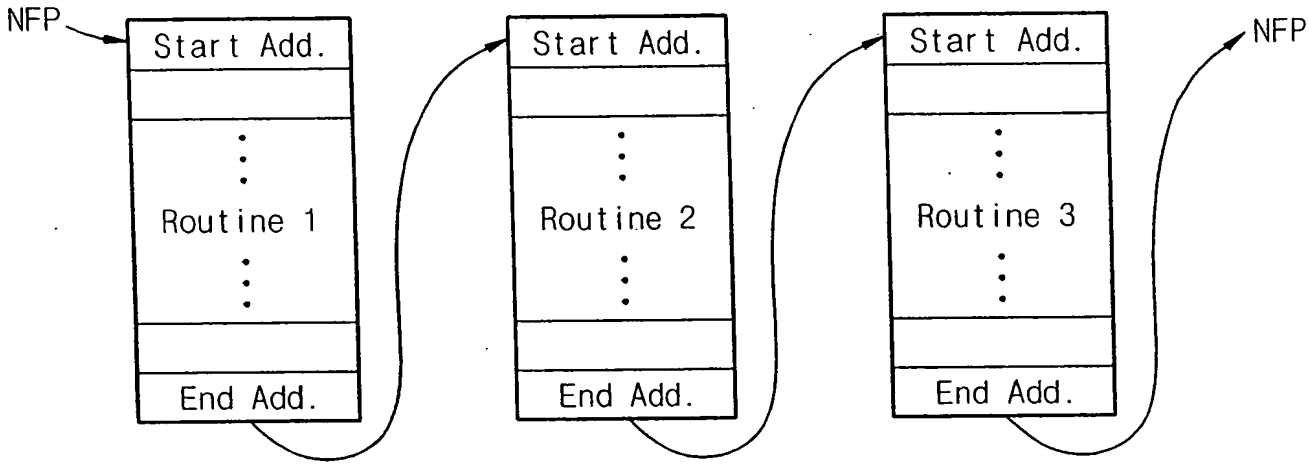

Fig. 9